R.G. Government Polytechnic Banikhet, Distt. Chamba (H.P)-176303

Department of Electrical Engineering

Lesson Plan

Name of Faculty	Ms. Divya
Discipline	Electrical Engineering
Semester	4th
Subject	Digital Electronics (L-4 Hrs./week)
Lesson Plan Duration	February – June 2023

Week	Topic	Theory
1st (14 Feb. – 21 Feb.)	1. Introduction	Analog Signal, Digital Signal, Difference between Analog & Digital Signal
2nd (22 Feb. – 28 Feb.)	2. Number System	Binary, Octal, & Hexadecimal number systems, Conversion from Decimal, Octal & Hexadecimal Systems to Binary System & Vice Versa.
3rd (01Mar. – 07 Mar.)	2. Number System	Binary Addition, Subtraction, Multiplication, Division, 1's and 2's compliment methods of subtraction. - Concept of code: 8421, BCD
4th (09 Mar. – 16 Mar.)	3. Logic Gates & Families	Logic symbol, logical expression and truth table of AND, OR, NOT, NAND, NOR, EX- OR gates Universal property of NAND and NOR gate. - Logic Simplification Circuits
5th (17 Mar. – 23 Mar.)	3. Logic Gates & Families	Basic laws of Boolean algebra, Duality theorem, De Morgan's Theorems. - Boolean expressions using Sum of Products (SOP) and Product of Sums (POS) forms.
Class Test – 1	In third week of March 2023	
6th (24 Mar. – 31 Mar.)	3. Logic Gates & Families 4. Arithmetic Circuits	K-map representation of logical functions. - Minimization of logical expressions using K-map (2, 3, 4 variables) Logic Gates & Families (SSI, MSI, LSI, VLSI, ULSI) Half Adder /Full Adder Circuit, their design and implementation
7th (01 Apr. – 10 Apr.)	4. Arithmetic Circuits	Half Subtracter /Full Subtracter Circuit, their design and implementation

8th (11 Apr. – 19 Apr.)	5. Decoder, Encoder, Multiplexer & De-Multiplexer	Basic binary decoder, Encoder- Decimal to BCD Encoder
9th (20 Apr. – 27 Apr.)	5. Decoder, Encoder, Multiplexer & De-Multiplexer	Block diagram, Truth table, Logical expression and logic diagram of Multiplexers (4:1 and 8:1). Block diagram and Truth table of Demultiplexer (1:4 and 1:8)
10th (28 Apr. – 04 May)	6. Flip Flops, Counters, Shift-Registers	One-bit memory cell, clock signal, Latch-SR Latch, Difference between Latch & FlipFlop: S-R Flip flop, D- Flip Flop, J-K Flip Flop
11th (06 May – 12 May)	6. Flip Flops, Counters, Shift-Registers	Master Slave Flip-Flop, T- Flip Flop Counters: Asynchronous Counters/Ripple Counter (2 bit, 3-bit, Decade) : Synchronous Counters (2-bit, 3-bit, decade synchronous counter), Ring Counter
Class Test - 2	In third week of April 2023	
12th (15 May – 20 May)	6. Flip Flops, Counters, Shift-Registers	Shift Registers: Concept of Shift registers, Types of Shift registers (SISO, SIPO, PISO, PIPO and Universal Shift Registers) - Applications of Flip-Flops, Counters & Shift Registers
13th (23 May-29 May)	7. Memories 8. D/A & A/D Converters	Classification of Memories RAM, ROM, PROM, EPROM, E2PROM Digital to Analog Converters (Weighted register, R-2R Ladder D/A Converter)
House Test	In 2nd week of May 2023	
14th (30 May-05 June)	8. D/A & A/D Converters	Analog to Digital Converter (Dual Slope method, Successive Approximation A/D Converter) - Applications of A/D & D/A Converter
15th (06June – 09 June)	Revision & Doubt clearance	Revision & Doubt Clearance

NOTE: - Lesson Plan is Tentative, subject to availability of Time, Students & Faculty.

Signature of Teacher
(Er. Divya)

Signature of HOD/OIC
(Er. Amit Attri)